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ABSTRACT

The invention relates to the formation of structures in microelectronic devices such as integrated circuit devices by means of borderless via architectures in intermetal dielectrics. An integrated circuit structure having a substrate, a layer of a first dielectric material on the substrate; and spaced apart metal contacts on the layer of the first dielectric material. There is a space between adjacent metal contacts and each space is filled with the first dielectric material. A recess is formed in the filled spaces of the first dielectric material which extends from a level at a top of the metal contacts a part of the distance toward the substrate. A second dielectric layer is on at least some of the metal contacts and in the recesses on the filled spaces of the first dielectric material such that there is optionally a gap in the recesses of the second dielectric layer at side walls of the metal contacts. An additional layer of the first dielectric material is on the second dielectric layer. Vias extending through the additional layer of the first dielectric layer and the second dielectric layer extending to the top of at least some of the metal contacts and optionally to the gaps. The first dielectric material and the second dielectric material have substantially different etch resistance properties.